SYNTHESIS AND ELECTROPHYSICAL PROPERTIES OF CdS/ZnTe HETEROJUNCTIONS

Ion Lungu[1], Lidia Ghimpu[2], Lyudmila Gagara[1], and Tamara Potlog[1]

[1] *Moldova State University, str. A. Mateevici 60, Chisinau, MD-2009 Republic of Moldova*
[2] *Ghitu Institute of Electronic Engineering and Nanotechnologies, str. Academiei 3/3, Chisinau, MD-2028 Republic of Moldova*
**E-mail: ionlungu.usm@gmail.com*

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Abstract

In this paper results of studying CdS/ZnTe heterostructures synthesized by the quasi-closed space sublimation method on glass substrates coated with an ITO layer are described. The electrical and photoelectric properties of the structures are studied using current–voltage and capacitance–voltage characteristics in a temperature range of 30–100 °C. Analysis of the experimental data shows that the main specific feature of CdS/ZnTe structures is the formation of a high-resistance transition layer, which affects the separation of carriers at the barrier contact. The current carrier concentration in the space charge region, which is determined from the capacitance–voltage characteristics, is 1×10^{15} cm^{-3}; this fact suggests that one of the contacting materials—ZnTe—exhibits a high resistivity. Measurements of current–voltage characteristics in the solar cell mode give the following photoelectric parameters: open circuit voltage (U_{OC} = 0.53 V, J_{SC} = 27–30 μA/cm^2, and FF = 0.25.

Keywords: quasi-closed space sublimation method, diffraction patterns, current–voltage characteristics, capacitance–voltage characteristics, solar cells.

Rezumat

In aceasta lucrare sunt descrise rezultatele studierii heterostructurilor CdS/ZnTe sintetizate prin metoda sublimării în spațiu cvasi-închis pe substraturi de sticlă acoperite cu un strat de ITO. Proprietățile electrice și fotoelectrice ale structurilor au fost studiate folosind caracteristicile curent–tensiune și capacitate–tensiune în intervalul de temperatură de 30–100°C. Analiza datelor experimentale indică că principala caracteristică specifică a structurii CdS/ZnTe este formarea la interfață a unui strat de tranziție de înaltă rezistență, care afectează separarea purtătorilor de sarcină electrică. Concentrația impurităților purtătorilor ionizați în regiunea de sarcină determinată din caracteristicile capacitate–tensiune, constituie 1×10^{15} cm^{-3}; acest fapt sugerează că unul dintre materialele în contact, și anume ZnTe are o rezistivitate mai ridicată.

Măsurătorile caracteristicilor curent–tensiune în regim de celulă solară arată următorii parametri fotovoltaici: tensiunea de circuit deschis *(*U_{OC})= 0.53 V, densitatea curentului de scurt circuit (J_{SC}) = 27–30 μA/cm^2 și factorul de umplere (*FF)* = 0.25.
Cuvinte cheie: metoda volumului cvasi-închis, difracția de raze X, caracteristica curent–tensiune, caracteristica capacitate–tensiune, celulă solară

1. Introduction

A^2B^6 compounds are widely known as materials exhibiting fairly high photosensitivity for the entire visible spectrum of solar radiation; therefore, most of these compounds are commonly used for designing thin-film solar cells. A distinctive feature of these compounds is their pronounced monopolarity; therefore, these materials are used mostly in the form of heterojunctions. The best known thin-film heterojunction solar cells are those made of CdS/CdTe. However, the possibility of designing other pairs of heterojunction systems based on A^2B^6 compounds and solar cells based on these systems, in particular, CdS/ZnTe, is of interest [1, 3–7]. The theoretically calculated model of a CdS/ZnTe junction [2, 3] for an optimum ZnTe thickness of 2 μm gives an efficiency value of 10%, an open-circuit voltage (U_{OC}) of 1.81 V, and a short-circuit current density (J_{SC}) of up to 7 mA/cm^2 at a current–voltage characteristic (CVC) fill factor of 78.84%. The authors of [3] argue that, in terms of physical parameters, zinc telluride is one of the suitable semiconductors from A^2B^6 compounds for the development of low-cost and high-efficiency thin-film solar power engineering. Since the crystalline perfection of the semiconductor layers that form the structure is not mandatory, inexpensive synthesis techniques can be used. These layers can be formed at lower temperatures than those required for the formation of layered CdTe. Oxygen doping of zinc telluride layers leads to a decrease in the ZnTe band gap to 1.56 eV [7] and thereby makes it a fairly promising material for solar power engineering [8].

2. Synthesis Technique

A technology for synthesizing CdS layers by the quasi-closed space sublimation method was developed earlier for CdS/CdTe junctions. The required thicknesses were determined; the transmission and electrical parameters of the layers were measured [11].

The cadmium sulfide source was a CdS powder with a semiconductor grade purity of 99.9%. The evaporator temperature (T_E) of 590 ℃ provided the required density of the incident atomic flux. The substrate temperature (T_S) was varied in a range of 240–380 ºC; the thickness of the layers was controlled according to the time of formation of the layers and amounted to 0.5–0.7 μm. A CdS layer was deposited on a glass substrate with a thin indium tin oxide (ITO) layer by the quasi-closed space sublimation method. After that, the substrate was transferred to the zone of formation of a ZnTe layer, and a ZnTe layer was deposited also by the quasi-closed space sublimation method. The deposition temperatures for the ZnTe layer were chosen so that to hinder the reevaporation of the CdS layer. Thus, ZnTe layers were formed at T_S = 320 ℃ and T_E = 590 ℃. The thickness of the layer was controlled according to the time of formation, while providing the absence of visible violations of the layer continuity. The thickness of the layer was varied in a range of 4–8 μm. The ohmic contact to the ZnTe layer was made of thin layers of Ag, the work function of which is 4.7 eV; the Ag layers were deposited by vacuum evaporation.

3. Research Results

The crystal structure and phase composition of the films were studied at room temperature on a Bruker D8 X-ray diffractometer using CuK_α radiation (λ = 1.5406 Å, 40 mA, 40 kV) in a 2θ angular range of 10°–90°. The determined interplanar spacing values were compared with the reference values from the database [12]. X-ray diffraction patterns of thin CdS layers deposited on ITO/glass are shown in Fig. 1. The films have a polycrystalline structure, as evidenced by the reflection half-widths that are characteristic of polycrystalline substances. In the above specified range of diffraction angles, ITO peaks, in addition to the CdS peaks, were detected. X-ray diffraction analysis shows that an increase in T_S from 240 to 380 °C leads to a decrease in the intensity of the reflection of the (H102) plane, while the intensity of the line corresponding to the (H002) reflection plane increases. This relationship can indicate a reorientation of the crystals from the preferred (H102) plane to the (H002) plane. Thus, the CdS films are of a hexagonal modification and are textured in the [1002] direction.

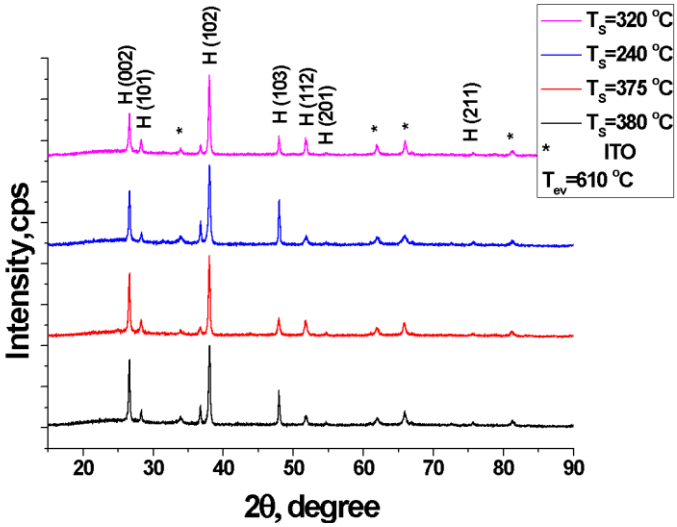

Fig. 1. X-ray diffraction patterns of the CdS/ITO layers.

Table 1 shows the structural characteristics of the CdS films deposited on ITO/glass, which were determined from the intense (H102) peak, and their dependence on T_S. According to the X-ray diffraction theory, the intensity of diffraction reflections is proportional to the square of the crystallite size; however, the reflection half-width is proportional to the first power of the crystallite size. Thus, the decrease in the intensity of the reflections with an increase in the T_S value of the films, to the first approximation, can be attributed to a decrease in the crystallite size, as evidenced by Table 1. The increase in the crystallite sizes slows down at T_S = 380 °C, while lattice strain increase. Lattice strain due to the imperfection and deformation of the crystal was calculated by the following formula:

$$\varepsilon = \frac{\beta_{hkl}}{tan\theta},$$

where β_{hkl} *is* full width at half maximum of diffraction peaks, θ is angle to the diffracting

planes.

The plane spacing equation for the hexagonal structure is:

$$\frac{1}{d^2} = \frac{4}{3}\left(\frac{h^2 + hk + k^2}{a^2}\right) + \frac{l^2}{c^2},$$

where a and c - lattice parameters of the unit cell and hkl - the Miller indices.

According to the published data, the parameters of the hexagonal crystal lattice of the CdS layers are as follows: a = 4.1307 Å, b = 4.1307 Å, and c = 6.7049 Å [2]; these values are in good agreement with the data in Table 1. The results of calculating the diffraction patterns are shown in Table 1.

Table 1. Microstructure parameters of CdS layers grown by the quasi-closed space sublimation method

Substrate temperature, °C	Intensity for the CdS peaks, cps	Crystallite size, Å	Lattice parameters			Lattice strain, ε
			a, Å	*b*, Å	*c*, Å	
240	554	436	4.1307	4.1307	6.7049	0,00413
320	502	329	4.1307	4.1307	6.7049	0,00357
375	413	349	4.1274	4.1274	6.7011	0,00362
380	365	307	4.1336	4.1336	6.7054	0,00377

The structure formed as a result of technological procedures is schematically shown in Fig. 2.

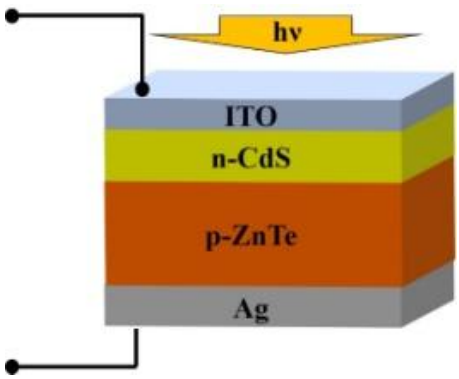

Fig. 2. Schematic representation of the synthesized ZnTe/CdS heterojunction.

The electrophysical properties of the structures formed in the described mode were studied. The CVC measurements in a temperature range of 30–100 °C showed that the current exhibits an exponential dependence on applied voltage in a region of up to 1.6 V (Fig. 3); it can be approximated by the following expression:

$$I = I_0\left(exp\left(\frac{eV}{nkT}\right) - 1\right). \quad (1)$$

where I_o is the reverse current of the *p*–*n* heterojunction, *q* is the electron charge ($q = 1.6 \times 10^{-19}$ C), *k* is the Boltzmann constant ($k = 1.38 \times 10^{-23}$ J deg), and *T* is the temperature (K),

n-ideality factor. A graphical representation of this dependence is shown in Fig. 3a. The CVC exhibits a pronounced nonlinearity, which is responsible for the dependence of the diode resistance on the operating-point position. Thus, a CdS/ZnTe barrier structure was formed. The empirically determined value of the barrier formed in this junction was 0.74–0.64 V for the given temperature range. The area of the measured samples was 0.25–0.4 cm^2.

The CVC was replotted in the ln*I* = *f*(*U*) coordinates (Fig. 3b) to determine the saturation currents in the studied temperature range, which are responsible for the quality of the heterojunction. The saturation current values for the given temperature interval and the change in the contact potential difference with a variation in temperature were empirically determined from ln*I* = *f*(*U*). All the data are summarized in Table 2.

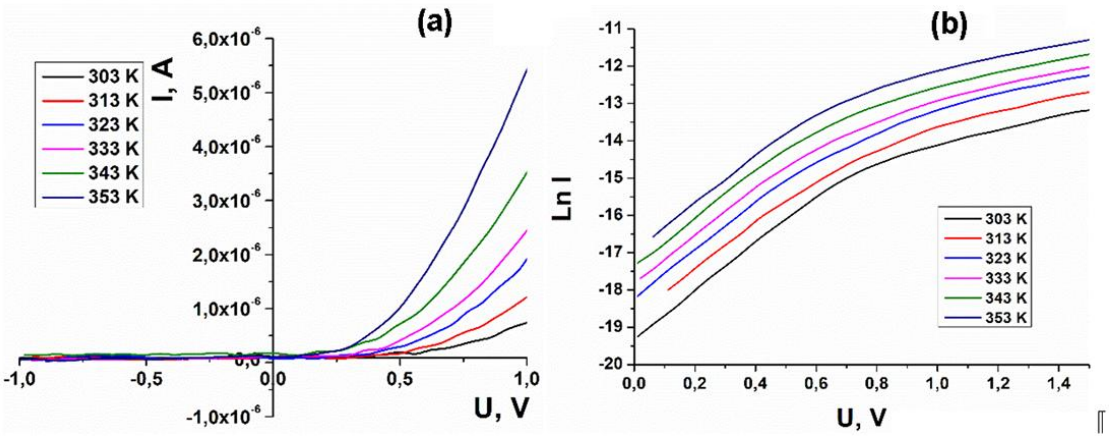

Fig. 3. Current–voltage characteristics of the CdS/ZnTe heterojunctions in a temperature range of 30–80 °C.

Table 2 summarizes the electrical parameters of the CdS/ZnTe structure calculated from the CVCs.

Table 2. Electrical parameters of the CdS/ZnTe structure

T_{meas}, K	I_0, A	U_d, V	*n* (Eq. (1))	R_s, kΩ
303	4.07×10^{-9}	0.74	7.27	560
313	6.98×10^{-9}	0.70	7.21	400
323	1.19×10^{-8}	0.69	6.61	250
333	1.82×10^{-8}	0.66	6.26	180
343	2.95×10^{-8}	0.65	6.22	180
353	4.18×10^{-8}	0.64	6.39	80

The capacitance–voltage methods for measuring the parameters of semiconductors were based on determining the dependence of the capacitance of a structure, which is attributed to the presence of a space charge in the near-surface region of the semiconductor, on the voltage applied to the structure. Capacitance–voltage (*C*–*V*) characteristics of the CdS/ZnTe

heterojunctions were studied in a temperature range of 30–80 °C. All measurements were conducted at a frequency of 1.5 MHz; the sample area was 0.25 cm^2. Figure 4 shows an equivalent circuit of a CdS/ZnTe heterojunction [10].

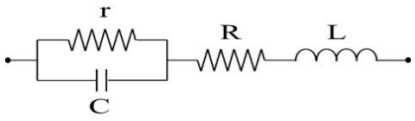

Fig. 4. Equivalent circuit of a CdS/ZnTe heterojunction; here, *r* is the internal resistance of the ZnTe layer; *R* is the series resistance of the entire CdS/ZnTe structure, which includes the contact resistance; *C* is the internal capacitance of the structure; and *L* is the inductance of the structure.

A characteristic feature of the *C–V* characteristics of CdS/ZnTe heterojunctions is the presence of a depletion region in a range of 0.80–0.55 V, after which the curves transit into a saturation region. The appearance of a saturation region in the *C–V* characteristic is typical for the presence of a high-resistance layer at the interface between two semiconductors [13]. The thickness of this transition layer was determined in accordance with the following expression:

$$d = \frac{\varepsilon_0 \varepsilon_{ZnTe} S}{C}, \tag{2}$$

where *d* is the thickness of the space charge region, ε_0 is the vacuum constant of 8.85 × 10^{-14} F/cm, ε_{ZnTe} = 10.1 is the dielectric permeability of ZnTe, and *S* (0.4 cm^2) is the area of the heterojunction. The thickness of this layer was 0.73–0.80 μm depending on measurement temperature. These layer thicknesses in the space charge region indicate the formation of a high-resistance region at the interface between the two semiconductors due to the mutual diffusion of the structure components or broken bonds of the atoms of the contacting materials. The thickness and properties of this layer depend on the technological parameters of the formation of a given structure, the doping level, and the choice of the doping component to decrease the resistance of ZnTe. It is difficult to determine parameters of this layer, because they can be states at the interface between two semiconductors and the resulting boundary states that fix the Fermi level at the interface in the heterojunction.

The replotting of these dependences in the $C^{-2} = f(U)$ coordinates (Fig. 5a) shows the presence of a wide region of a linear dependence of C^{-2} on applied voltage; for this region, a relationship for calculating the ionized impurity concentration in the space charge region can be used; in this case, it is true of the ZnTe component [9], because the calculation of the resistance of the CdS layers during formation showed that their resistivity is 2 × 10^{-3} to 4 × 10^{-3} Ω cm. The resistance of the ZnTe layers calculated from the direct CVCs was 2 × 10^5 to 4 × 10^5 Ω. This fact suggests that the space charge region is entirely localized in the ZnTe layer:

$$N_{ef} = \frac{2\Delta U}{q\varepsilon_0 \varepsilon_{ZnTe} S^2 \Delta\left(1/C^2\right)}. \tag{3}$$

Figure 5 shows $C^{-2} = f(U)$ dependences of the CdS/ZnTe structures measured at 40 °C (Fig. 5a) and in a temperature range of 30–80 °C (Fig. 5b).

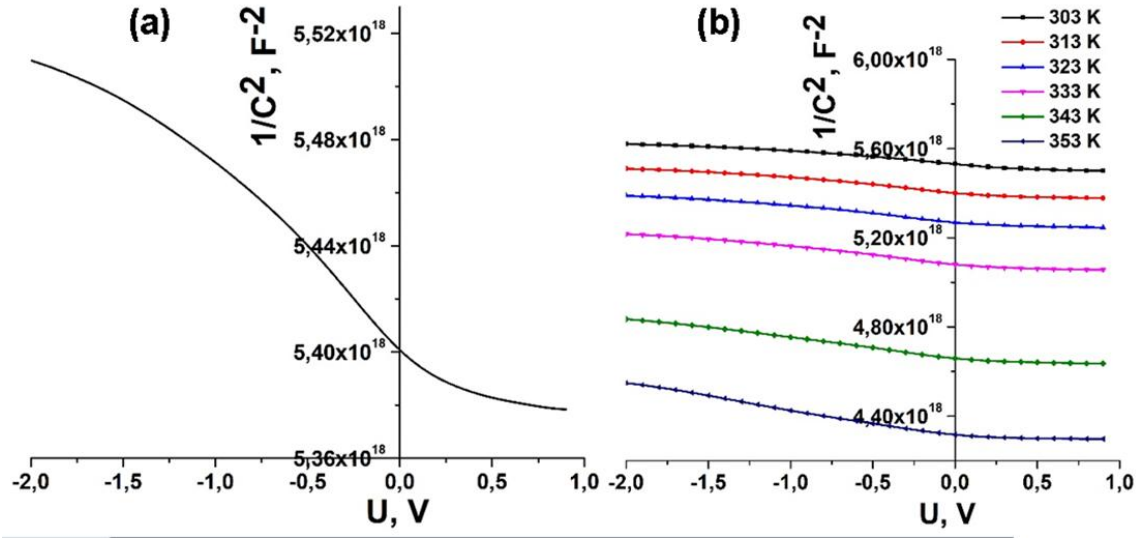

Fig. 5. $C^{-2} = f(U)$ dependences of the CdS/ZnTe heterojunction measured (a) at 40 °C and (b) in a temperature range of 30–80 °C.

According to the calculations, from the $C^{-2} = f(U)$ dependence for a temperature range of 30–80 °C, the ionized impurity concentration in the space charge region of the structure was determined to be 0.61×10^{14} to 1.0×10^{14} cm^{-3}. Low charge carrier concentrations suggest that the ZnTe component of the structure and the transition layer exhibit high resistivity. The contact potential difference value determined from the *C–V* characteristics in this structure was $U_d = 0.68$ V; this value is in good agreement with the values determined from the CVCs.

The structures were irradiated with integral light with an intensity of 100 mW/cm^2. Figure 6 shows that the open-circuit voltage is $U_{OC} = 0.53$ V, while the short circuit current density is $J_{SC} = 27–30$ μA/cm^2. The CVC fill factor is $FF = 0.25$. Low CVC fill factor values also support the conclusion that a high-resistance transition region is formed at the interface between two contacting semiconductors and, together with the high resistance of the heterojunction material, indicate a high series resistance of the entire structure, which, in turn, leads to low energy parameters of this barrier structure.

Table 3. Photoelectric parameters of the CdS/ZnTe heterojunction in the solar cell operating mode

Silver contact	I_{SC}, μA	U_{OC}, V	FF, %	R_S, kΩ	R_{sh}, MΩ
sprayed	12	0.44	14.3	54	80
paste	43	0.53	25.1	30	6

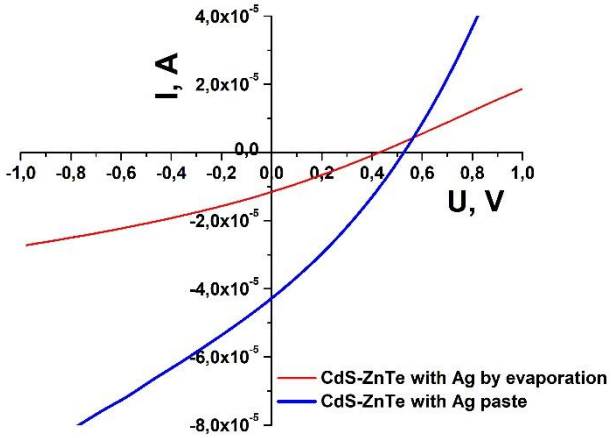

Fig. 6. Current–voltage characteristics of the CdS/ZnTe heterojunction in the solar cell mode.

Based on the results obtained, we assume that CdS/ZnTe is an anisotype heterojunction with an intermediate layer, because to provide the absence of defects in the crystal lattice of the two materials constituting the heterojunction, the materials should at least have an identical crystalline structure and similar lattice constants. Figure 7 shows the energy diagram of a CdS/ZnTe heterostructure in thermodynamic equilibrium, which was constructed in terms of the Donnelly and Milnes model [14].

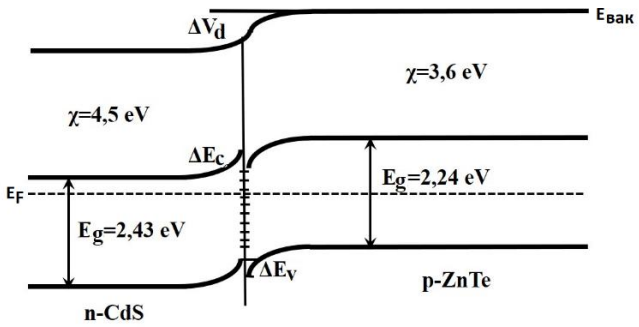

Fig. 7. Assumed energy diagram of a CdS/ZnTe heterojunction in thermodynamic equilibrium.

The composition of the metallurgical layer at the interface between two contacting semiconductors cannot be determined; it can be assumed that this layer is formed due to the diffusion of the ZnTe/CdS heterojunction components.

4. Conclusions

- CdS/ZnTe heterostructures have been synthesized by the quasi-closed space sublimation method.

- The electrical characteristics of the synthesized CdS/ZnTe heterojunction have been studied and their main electrical parameters U_{OC}, I_{SC}, and R_S have been calculated.
- According to the results of studying the *C–V* characteristics, it has been shown that a high-resistance layer is formed at the interface between the CdS and ZnTe layers; this layer, together with the fairly high resistance of ZnTe, is responsible for the low parameters of the structure in the solar conversion mode.
- The energy parameters of the CdS/ZnTe heterojunction have been measured. The low values of the energy parameters are characterized by a high series resistance, the determining role in which is played by both the intermediate layer and the high resistance of ZnTe as the main absorbing component.
- According to the experimental results, an energy diagram of the studied heterojunction has been proposed. Either the composition or the degree of interaction of the formed intermediate layer cannot yet be determined; the only assumption that has been made in this respect is that the thickness and properties of this layer depend on the technological parameters of the synthesis of this structure, the doping level, and the choice of the doping component to decrease the resistance of ZnTe.

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Information about the authors:

Ion LUNGU, postgraduate student of the Doctoral School of Physical and Engineering Science, researcher at the Laboratory of Organic/Inorganic Materials in Optoelectronics; Moldova State University
E-mail: ionlungu.usm@gmail.com
ORCID: 0000-0002-7117-672X

Lydia GHIMPU, Dr., Director of the Institute of Electronic Engineering and Nanotechnologies of Moldova

Lyudmila GAGARA, Dr., Senior Researcher, Laboratory of Organic/Inorganic Materials in Optoelectronics; Moldova State University
E-mail: lgagara2019@mail.ru

Tamara POTLOG, Assoc. Prof., Dr., Head of the Laboratory of Organic/Inorganic Materials in Optoelectronics; Moldova State University
E-mail: tpotlog@gmail.com
ORCID: 0000-0003-1243-9371